

# Research Snapshots 2018-19

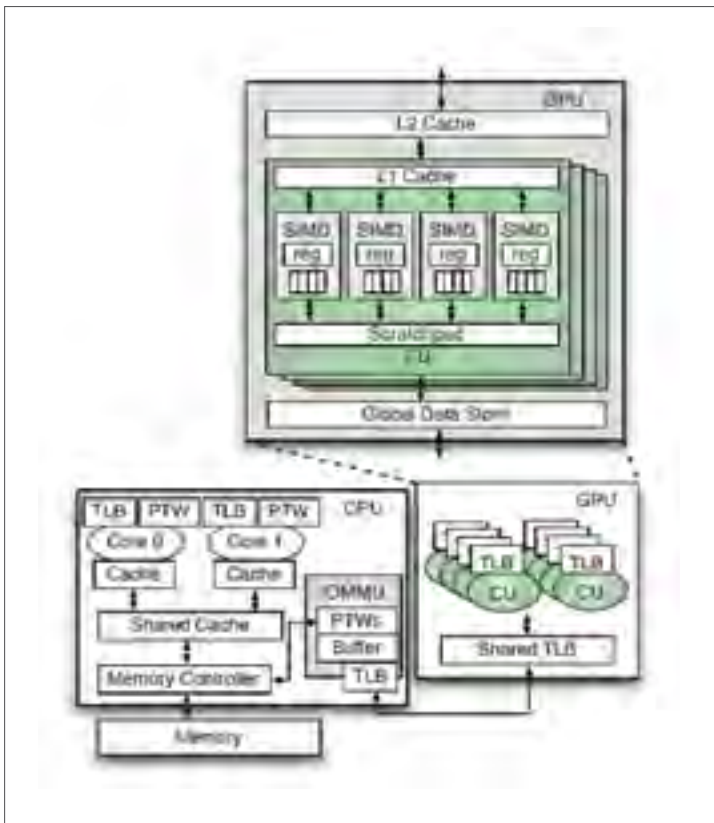


## P V Kumar (ECE)

Ensuring reliable communication with low latency, is key to next-generation applications such as interactive voice and video, multiplayer gaming, multiplayer virtual reality and telesurgery. Not surprisingly, ultra-reliable low-latency communication is one of three focus areas of 5G cellular systems.

Our group has recently come up with a class of low-complexity, packet-level forward error-correction codes, termed as streaming codes. These codes maximize the rate of information transmission while maintaining robustness against a large class of packet-erasure patterns, under a stringent decoding-delay constraint. The packet erasures could arise for example, from dropped packets due to congestion in the network, or packets that are lost on account of a wireless link that is experiencing a deep fade. Our work has received recognition in the form of a paper [2] that was one of four finalists for the 2019 IEEE Jack Wolf ISIT Student Paper Award. It was also awarded a Qualcomm Innovation Fellowship 2019, India [3].





## Arkaprava Basu (CSA)

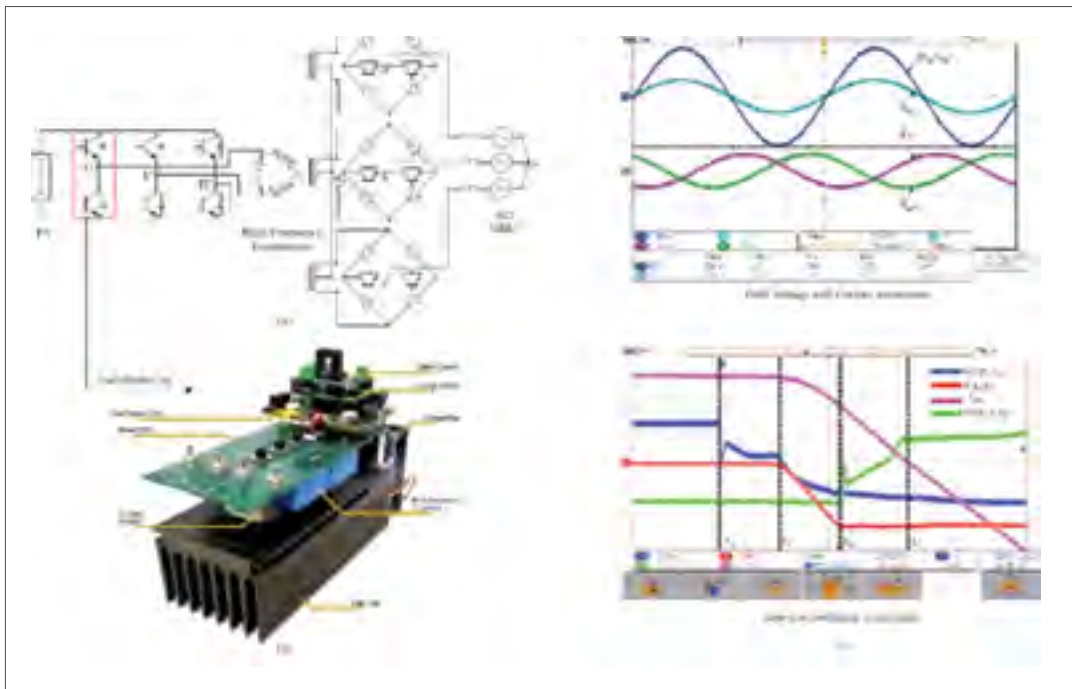
Traditionally, the Central Processing Unit or CPU has been the brain of a computer. In recent times, however, Graphics Processing Unit or GPUs are emerging as a platform of choice for massively parallel computations, such as deep learning. But, writing a program for GPU is significantly harder than writing one for the CPU. Further, while a significant fraction of modern computing today happens in the public cloud computing infrastructures (e.g., Amazon’s EC2), GPUs are not easy to deploy to the cloud. These present significant predicaments in fully harnessing compute capabilities of modern GPUs.

Arkaprava and his team’s focus has been to make GPUs more easily programmable and deployable in the cloud platforms through co-design of the hardware and the software. More recently, they are working on how the hardware can provide feedback to the programmer to help her to write correct GPU programs.

Arkaprava Basu, Eric Van Tassell, Mark Oskin, Guilherme Cox, Gabriel Loh. “Single instruction multiple data page table walk scheduling at input output memory management unit”. US Patent App. 15/852,442, 2019.

Seunghee Shin, Michael LeBeane, Yan Solihin, and Arkaprava Basu. “Neighborhood-aware address translation for irregular GPU applications”. In Proceedings of the 51st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-51). Fukuoka, Japan – October 20 - 24, 2018, pp 352-363.





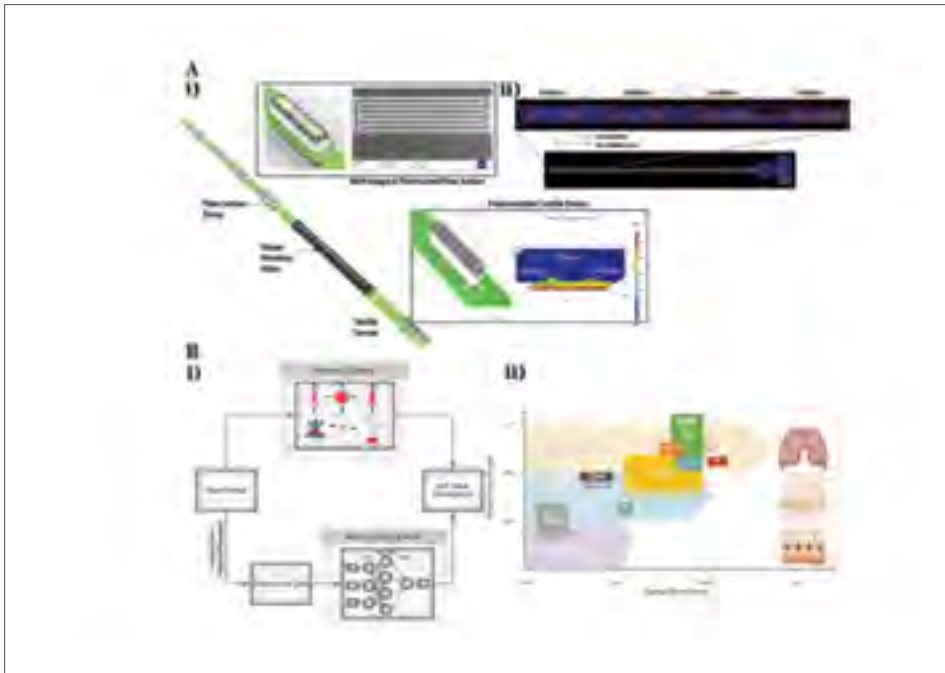
### Kaushik Basu (EE)

Solar power being one of the most promising sources of renewable energy in our country, past few years witnessed rapid integration of utility scale solar into our power grid with a target of 100GW of solar capacity by 2022. A DC to AC power electronic converter, also known as an inverter, followed by a transformer is used to interface PV panels with the grid. Transformer is necessary for safety and to protect the panels from the damage due to leakage current. This transformer, operating at grid frequency of 50Hz, is one of the most expensive and heaviest components in the power conversion unit. It is well known, that size of a transformer is inversely proportional to the frequency of operation. One of the known ways to address this problem is to employ a DC-DC converter that incorporates a high frequency transformer, followed by an inverter. This so-called multi-stage solution has difficulty due to higher power loss in the semiconductor devices and presence of a large electrolytic capacitor at the interconnection of the two stages (DC-DC and DC-AC), compromising reliability. Our recent work on DC-AC converters with a high frequency transformer has shown that it possible to eliminate this capacitor through a single-stage, more silicon approach, improving reliability. Suggested, high frequency link inverter solutions practically result in minimum switching loss in power devices. As the loss is decoupled with frequency, the transformer size can be further reduced. Our target designs show that the proposed methods achieve efficiency comparable with the state-of-the-art solution, but at fraction of its size and cost.

Pal A, and Basu K, A Unidirectional Single-Stage Three-Phase Soft-Switched Isolated DC-AC Converter. *IEEE Transactions on Power Electronics*, Vol: 34, Issue: 2, Feb. 2019.

Pal A, and Basu K, A Soft-switched High Frequency link Single-Stage Three-Phase Inverter for Grid Integration of Utility Scale Renewables. *IEEE Transactions on Power Electronics*, Vol: 34, Issue: 9, Sept. 2019.





### Hardik J Pandya (DESE)

The Advanced Microsystems and Biomedical Devices Facility for Clinical Research and Biomedical & Electronic (10-6-10-9) Engineering Systems Laboratory lead by Hardik J. Pandya is developing innovative healthcare technologies integrating biology/medicine with microtechnology, nanotechnology, electronic systems, and additive manufacturing to solve unmet clinical problems. Chronic inflammation of the upper airway in infants is often life-threatening and can result in a variety of diseases such as asthma, airway obstruction or hyper reactive airway diseases. Common symptoms include recurrent stridor, chronic cough, cyanotic episodes, feeding difficulties, recurrent aspiration, pneumonia often affecting the ability to breathe and swallow. Management of tracheal malformations is complex and requires an individualized approach with timely diagnosis and treatment. The small airway in infants often has the potential to worsen the impact of airway disorders. Chronic airway and soft tissue inflammation cause progressive weakening of the airway walls resulting in destruction of the tracheal cartilaginous rings.

Efficient management of difficult airway calls for newer diagnostic tools as well as development of innovative management techniques enabling a better prognosis. We present a novel, easily reproducible tool for quantitative assessment of the tissue mechanical property and simultaneously measure airflow in challenging airway- a valuable guide to surgical therapy based on precise, objective data.

This work was done in collaboration with Clinical Collaborators Dr. Sanjay Rao, Senior Consultant and Head, Department of Pediatric Surgery, Mazumdar Shaw Multispecialty Hospital.

Aleky, B., Sanjay Rao, and Hardik J. Pandya. "Engineering approaches for characterizing soft tissue mechanical properties: A review." *Clinical Biomechanics*, vol. 69, pp. 127–140, Oct. 2019.





### **Vinod Ganapathy (CSA) and Chiranjib Bhattacharyya (CSA)**

Commercial and end-user drones are becoming widely available. Such drones can be employed for a number of interesting and socially-beneficial use-cases, such as sensing, search and rescue, and product delivery. However, the wide availability of drones has also put a previously tightly-regulated resource, i.e., airspace, into the hands of commercial entities and end-users. We are already beginning to read about an increasing number of cases where commercial drones can pose dire risks., e.g. in the form of “near-misses” between drones and aeroplanes.

In this project, our focus is on the privacy risk posed by drones. Drones can capture pictures and video with their on-board cameras---in fact, this may be an essential part of navigating the drone. But as citizens on the ground, how do we get an assurance that these pictures and videos captured by third-party drones will not compromise our privacy? This problem is extremely challenging, primarily because the drone belongs to a third-party, e.g., it could be a delivery drone being operated by a delivery fleet operator.

At the Computer Systems Security Laboratory, we are developing techniques and tools to address this problem. We are developing the machinery by which (1) the host of a restricted space (e.g., the IISc campus, or an apartment complex), could specify a set of privacy policies that guest drones must comply, and (2) the guest drone can prove, using trusted hardware, to the host that it is in compliance. As our work matures, we hope to interact with and influence India’s emerging drone policies (e.g., Digital Sky).

Regulating Drones in Restricted Spaces, Abhishek Vijeev, Vinod Ganapathy, and Chiranjib Bhattacharyya, *Proceedings of HotMobile’19, the 20th International Workshop on Mobile Computing Systems and Applications*, Santa Cruz, California, USA, February 2019.







### **Vinod John (EE)**

Supplying power to rural and remote regions through single-phase distribution or microgrid is a preferred choice over a three-phase system, owing to cost benefits. Though, three-phase induction machines offer better torque and power density at a low cost as compared to their single-phase counterparts. The availability of only single-phase power limits the usage of three-phase induction motors in applications such as pumps, mills, cold-storage plants in the agricultural sector and machine tool industries in small urban and rural set-ups. Inexpensive power converters are adopted to achieve cost benefits at the expense of efficiency and power quality. In this context, many active phase converters (APCs) with fewer power electronic devices are proposed to reduce the converter size and cost. These APCs have limitation such as reduced life due to low-frequency current in the dc-link, high inrush currents while starting an induction motor, impact on motor bearing life due to converter generated voltage or increased system cost due to sine-filter at the output.

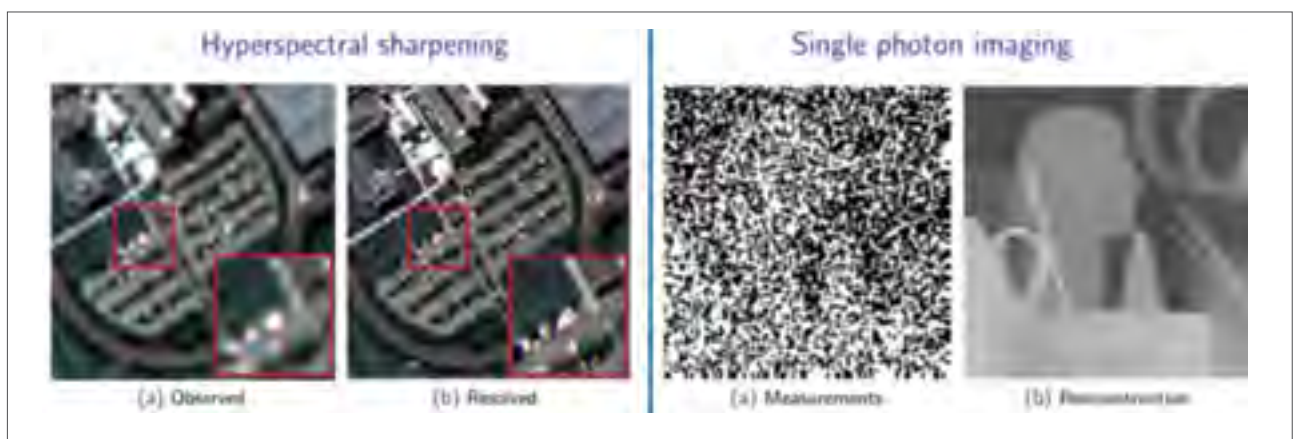
Research on an auxiliary capacitor assisted APC (AC-APC) address these challenges discussed above. The proposed AC-APC bypasses sufficient power from the grid to load, and process only a fraction of the load power, thus achieving low power converter ratings. This boosts the system efficiency and enhances the converter lifespan. The utility service provider also benefits as the AC-APC draw clean power and does not cause the harmonic distortions of a diode-bridge based converters, while having low reactive power consumption. Filtered voltages at the motor terminals enhances the motor life, which is achieved at low cost with a fewer number of filter components. This work also covers aspects such as regenerative operation which has potential use in small-scale hydel and biogas power plants, and is design to generate minimal electromagnetic noise interference.

This technology can boost the productivity of the agricultural sector. A centralized AC-APC can be used for irrigation, machinery in the agricultural fields, and compressor motors of the cold-storage plants. Typically, multiple small motors are used in a small-scale urban and rural industries, and the developed AC-APC can serve these applications as well.

Anil K Adapa and Vinod John, "An Auxiliary Capacitor Based Active Phase Converter with Reduced Device Current Stress," IEEE Trans. on Ind. Electron., Sept. 2019.

Anil K Adapa and Vinod John, "Reduced Rating Active Phase Converter for Three Phase Induction Generator based Single Phase Grid-Tied Systems," PEDES Conf., Dec. 2018.

"A Reduced Switch Count Active Phase Converter with Reduced Component Ratings", Indian Patent Appl. No. 201741028910, Filed on: Aug. 2018 (Indian Institute of Science, Central Power Research Institute (CPRI) and C-DAC,).

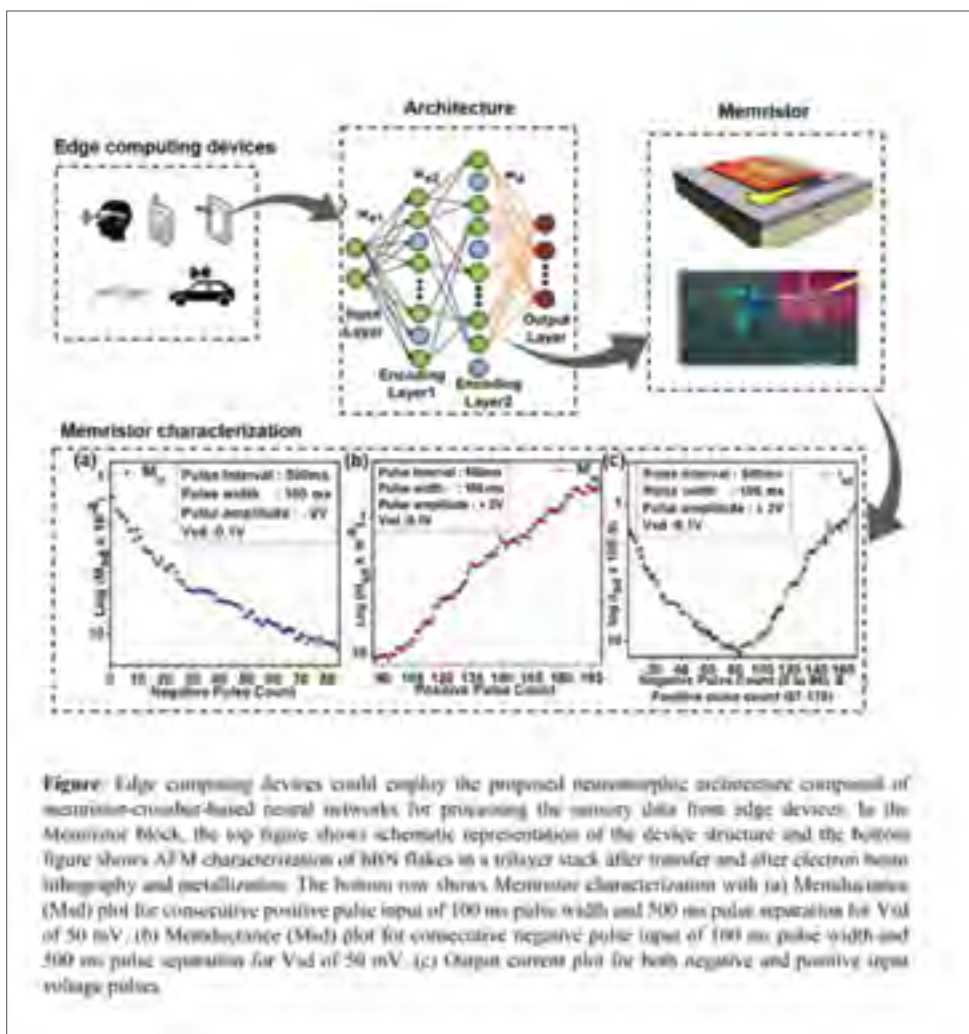


### K N Chaudhury (EE)

The quintessential computational problem in imaging modalities such as nuclear magnetic resonance imaging, x-ray tomography, microscopy, etc. is the reconstruction of high-resolution images from physical measurements. Dramatic progress has been made in the last couple of decades producing several powerful ground-truth priors that also yield fast numerical algorithms. Typically, the algorithms are based on iterative methods, where each iteration involves the inversion of the measurement model followed by enforcement of the ground-truth prior. More recently, researchers have come up with an ingenious means of enforcing priors, namely, the image after the inversion (during which artifacts are introduced) is cleaned up using a powerful image denoiser. This so-called plug-and-play paradigm involves the repeated inversion of the measurement model followed by the denoising step. Recently, we have come up with ways of speeding up plug-and-play algorithms (often by a couple of orders) using efficient image denoisers [1,2]; what would typically take minutes can now be done in few seconds. (joint work with Sanjay Ghosh, Unni VS, and Pravin Nair)

P. Nair, V. S. Unni, and K. N. Chaudhury. Hyperspectral image fusion using fast high-dimensional denoising. Proc. IEEE International Conference on Image Processing (ICIP), 2019.

V. S. Unni, S. Ghosh, and K. N. Chaudhury. Linearized ADMM and fast nonlocal denoising for efficient plug-and-play restoration. Proc. IEEE Global Conference on Signal and Information Processing (GlobalSIP), 2018.



### C S Thakur (DESE)

Neuromorphic systems are emerging as a promising promenade towards building the next generation of intelligent computational systems where intelligence is directly embedded onto small, low-power and computationally heavy hardware devices. Owing to the proliferation of internet-of-things (IoTs) in the areas of ubiquitous sensing, there has been an increased demand towards integrating intelligence directly onto edge devices or IoT hardware platform. The machine learning architecture embedded into these platforms needs to be as energy-efficient as possible. We developed a low-power CMOS-Memristor based hybrid architectural framework

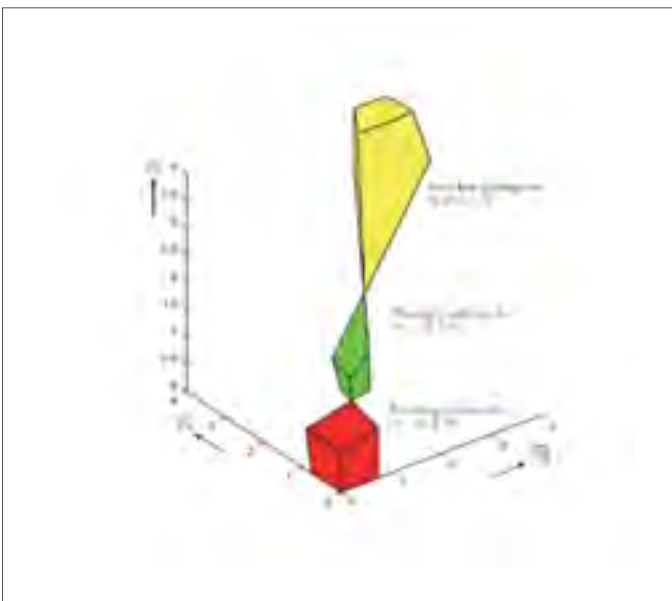


for edge computing devices, to enable intelligent data processing directly at the sensor nodes. The basic computational block, i.e., neuron, has been implemented using CMOS analogue circuit and the synaptic connectivity between neurons has been implemented using our novel low-power memristor device as an analogue memory in our cognitive computing framework. This memristor device was fabricated (in collaboration with Prof. Arindam Ghosh, Department of Physics, IISc) using a three-layer stack comprising an ultrathin single layer molybdenum disulphide (MoS<sub>2</sub>) as the channel, hexagonal boron nitride (hBN) as the dielectric, and an extended graphite floating gate. The power consumption of the basic CMOS computational block is 3nW in the 65nm process technology, while the energy consumption per cycle was 0.3pJ for potentiation and 20pJ for depression cycles of the synaptic memristor device during the training of the machine learning algorithms. The characteristics of the proposed CMOS-Memristor hybrid framework enable it to be employed in onsite processing of data such as in IoT devices, energy- and area-constrained devices.

T. Paul, T. Ahmed, K. K. Tiwari, C. S. Thakur, A. Ghosh, (2019) "A high-performance MoS<sub>2</sub> synaptic device with floating gate engineering for Neuromorphic Computing". *2D Material* (IOP Science).

P. Kumar, A. R. Nair, O. Chatterjee, T. Paul, A. Ghosh, S. Chakrabartty, C. S. Thakur, "Neuromorphic In-Memory Computing Framework using Memtransistor Cross-bar based Support Vector Machines." *IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019.

S. Gupta, P. Kumar, T. Paul, A. van Schaik, A. Ghosh, C. S. Thakur, "Low Power, CMOS-MoS<sub>2</sub> Memtransistor based Neuromorphic Hybrid Architecture for Wake-Up Systems" *Nature Scientific Reports* (In Final Stage), 2019.



### Siddharth Barman (CSA)

Fairness is a fundamental consideration whenever resources/goods have to be distributed among competing agents with equal entitlements, but distinct preferences. A substantive body

of work in Economics and Mathematics is aimed at quantitatively understanding fairness and establishing existential results. Such provable guarantees, and the accompanying framework, have guided the design of (fair) allocation policies in several contexts, such as border disputes and cloud computing environments. However, to be useful in practice, one also requires scalable methods that explicitly find the underlying fair allocations. Motivated by this consideration, the research group of Dr. Siddharth Barman have developed results that address algorithmic aspects of fair division.

Specifically, a recent work of the group [1] shows that, in a relevant context, economic efficiency is not sacrificed by imposing fairness. This work is conceptually surprising since it shows that the seemingly incompatible properties of fairness and economic efficiency can be achieved together. The result has practical implications since it carries with it an algorithm for finding allocations are that both fair and (Pareto) efficient.

Another joint work of Dr. Barman [2] addresses fairness in settings that entail resource sharing with monetary transfers. This setting has been studied in Microeconomics for over three decades and is referred to as fair rent division, since it captures (as a stylized example) the problem of fairly dividing an apartment's rent among the roommates. The result [2] provides the first efficient algorithm for this classic problem and relies on an interesting geometric insight: in this setup, even though the underlying "feasible set" is non-convex, it is always composed of a chain of convex sets (see appended Figure). Dr. Barman's group is also working towards Blockchain implementations of fair-division algorithms.

Eshwar Arunachaleswaran, Siddharth Barman, and Nidhi Rathi. *Fully Polynomial-Time Approximation Schemes for Fair Rent Division*. *ACM-SIAM Symposium on Discrete Algorithms (SODA)*, 2019.

Siddharth Barman, Sanath Krishnamurthy, and Rohit Vaish. *Finding Fair and Efficient Allocations*. *ACM Conference on Economics and Computation (EC)*, 2018.

